



## A5N:3200.XXH

Part Number	V <sub>RRM</sub> , V <sub>R</sub> (V) Max. rep. peak reverse voltage		V <sub>RSM</sub> , V <sub>R</sub> (V) Max. non- rep. peak reverse voltage
	T <sub>J</sub> = 0 to 125°C	T <sub>J</sub> = -40 to 0°C	T <sub>J</sub> = 25 to 125°C
	A5N:3200.02	200	200
A5N:3200.04	400	400	500
A5N:3200.06	600	600	700
A5N:3200.08	800	800	900
A5N:3200.10	1000	1000	1100
A5N:3200.12	1200	1200	1300
A5N:3200.14	1400	1400	1500
A5N:3200.16	1600	1600	1700

### MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T <sub>J</sub> Junction Temperature	-40 to 125	°C	-
T <sub>stg</sub> Storage Temperature	-40 to 150	°C	-
I <sub>F(AV)</sub> Max. Av. current @ Max. T <sub>C</sub>	3200	A	180° half sine wave
	70	°C	
I <sub>F(RMS)</sub> Nom. RMS current	5030	A	-
I <sub>FSM</sub> Max. Peak non-rep. surge current	58.7	KA	50 Hz half cycle sine wave Initial T <sub>J</sub> = 125°C, rated V <sub>RRM</sub> applied after surge.
	61.7		60 Hz half cycle sine wave
	69.5		50 Hz half cycle sine wave Initial T <sub>J</sub> = 125°C, no voltage applied after surge.
	73		60 Hz half cycle sine wave
I <sup>2</sup> t Max. I <sup>2</sup> t capability	14614	kA <sup>2</sup> s	t = 10ms Initial T <sub>J</sub> = 125°C, rated V <sub>RRM</sub> applied after surge.
	15885		t = 8.3 ms
	20663		t = 10ms Initial T <sub>J</sub> = 125°C, no voltage applied after surge.
	22460		t = 8.3 ms
I <sup>2</sup> t <sup>1/2</sup> Max. I <sup>2</sup> t <sup>1/2</sup> capability	246050	kA <sup>2</sup> s <sup>1/2</sup>	Initial T <sub>J</sub> = 125°C, no voltage applied after surge. I <sup>2</sup> t for time t <sub>x</sub> = I <sup>2</sup> t <sup>1/2</sup> * t <sub>x</sub> <sup>1/2</sup> . (0.1 < t <sub>x</sub> < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	800	A/μs	T <sub>J</sub> = 125°C, V <sub>D</sub> = V <sub>DRM</sub> , I <sub>TM</sub> = 1600A. Gate pulse: 20V, 20Ω, 10μs, 0.5μs rise time, Max. repetitive di/dt is approximately 40% of non-repetitive value.
P <sub>G(M)</sub> Max. Peak gate power	16	W	tp < 5 ms
P <sub>G(AV)</sub> Max. Av. gate power	3.0	W	-
+I <sub>GM</sub> Max. Peak gate current	4	A	tp < 5 ms
-V <sub>GM</sub> Max. Peak negative gate voltage	15	V	-
F Mounting Force	4550	N.m	Non lubricated threads



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## CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$V_{TM}$ peak on-state voltage	---	1.43	1.54	V	Initial $T_J = 25^\circ\text{C}$ , 50-60Hz half sine, $I_{peak} = 10053\text{A}$ .
$V_{T(TO)1}$ Low-level threshold	---	---	0.899	V	$T_J = 125^\circ\text{C}$ Av. power = $V_{T(TO)} * I_{T(AV)} + r_T * [I_{T(RMS)}]^2$
$V_{T(TO)2}$ High-level threshold	---	---	0.719		
$r_{T1}$ Low-level resistance	---	---	0.065	m $\Omega$	Use low values for $I_{TM} < \pi$ rated $I_{T(AV)}$
$r_{T2}$ High-level resistance	---	---	0.052		
$I_L$ Latching current	---	270	---	mA	$T_C = 25^\circ\text{C}$ , 12V anode. Gate pulse: 10V, 20 $\Omega$ , 100 $\mu\text{s}$ .
$I_H$ Holding current	---	100	500	mA	$T_C = 25^\circ\text{C}$ , 12V anode. Initial $I_T = 10\text{A}$ .
$t_d$ Delay time	---	0.5	1.5	$\mu\text{s}$	$T_C = 25^\circ\text{C}$ , $V_D =$ rated $V_{DRM}$ , 50A resistive load. Gate pulse: 10V, 20 $\Omega$ , 10 $\mu\text{s}$ , 1 $\mu\text{s}$ rise time.
$t_q$ Turn-off time	---	---	100	$\mu\text{s}$	$T_J = 125^\circ\text{C}$ , $I_{TM} = 500\text{A}$ , $di/dt = 25\text{A}/\mu\text{s}$ , $V_R = 50\text{V}$ . $dv/dt = 200\text{V}/\mu\text{s}$ lin. To 80% rated $V_{DRM}$ . Gate: 0V, 100 $\Omega$ .
$dv/dt$ Critical rate-of-rise of off-state voltage	500	700	---	V/ $\mu\text{s}$	$T_J = 125^\circ\text{C}$ . Exp. to 100% or lin. Higher $dv/dt$ values available. To 80% $V_{DRM}$ , gate open.
	1000	---	---		
$I_{RM}$ , $I_{DM}$ Peak reverse and off-state current	---	80	200	mA	$T_J = 125^\circ\text{C}$ , Rated $V_{RRM}$ and $V_{DRM}$ , gate open.
$I_{GT}$ DC gate current to trigger	---	---	500	mA	$T_C = -40^\circ\text{C}$ $T_C = 25^\circ\text{C}$ +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
	75	150	250		
$V_{GT}$ DC gate voltage to trigger	---	---	3.3	V	$T_C = -40^\circ\text{C}$ $T_C = 25^\circ\text{C}$
	---	1.2	2.5		
$V_{GD}$ DC gate voltage not to trigger	---	---	0.3	V	$T_C = 25^\circ\text{C}$ , Max. Value which will not trigger with rated $V_{DRM}$ anode-to-cathode.
$R_{thJC}$ Thermal resistance, junction-to-case	---	---	0.011	$^\circ\text{C}/\text{W}$	DC operation.
	---	---	0.012	$^\circ\text{C}/\text{W}$	180 $^\circ$ sine wave, double side cooled.
	---	---	0.013	$^\circ\text{C}/\text{W}$	120 $^\circ$ rectangular wave, double side cooled.
$R_{thCS}$ Thermal resistance, case-to-sink	---	---	0.006	$^\circ\text{C}/\text{W}$	Mtg. Surface smooth, flat and greased.
wt Weight	---	1590 (56)	---	g(oz.)	---
Case Style	TO-200AE			JEDEC	---

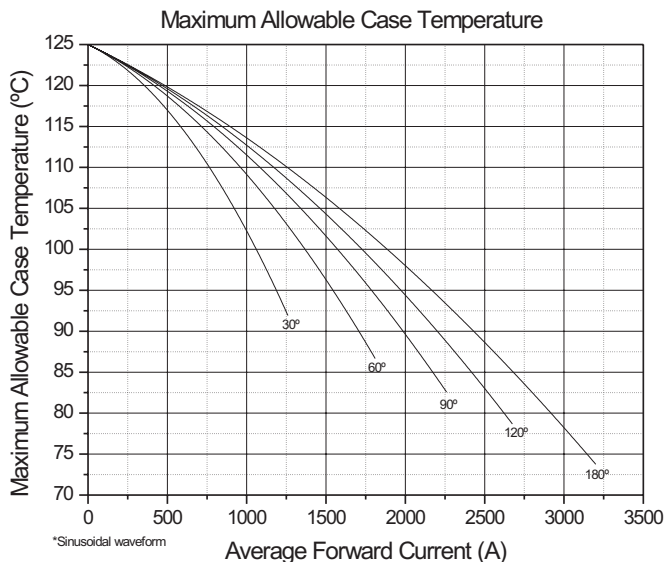


Fig. 1 - Current Ratings Characteristics

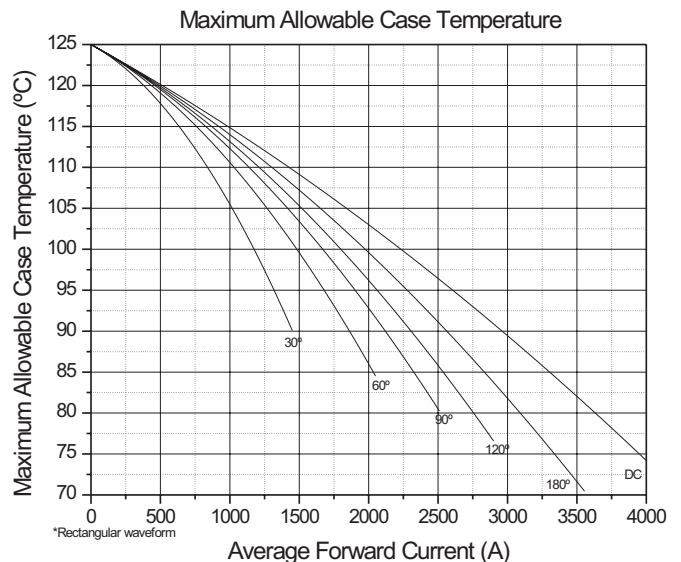


Fig. 2 - Current Ratings Characteristics



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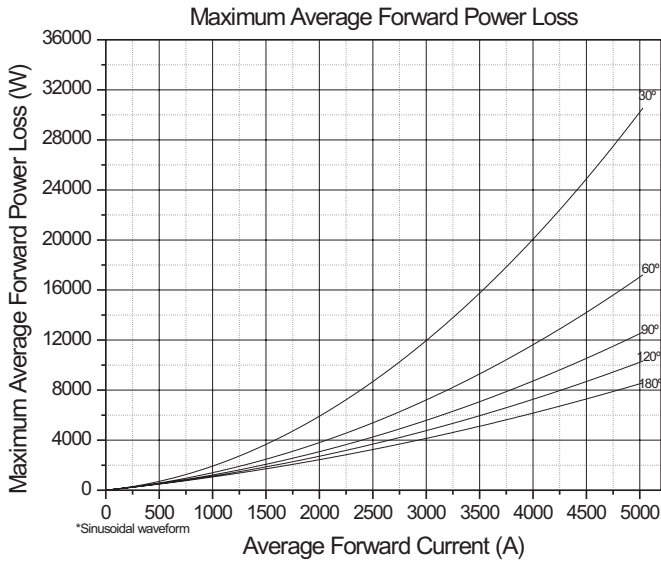


Fig. 3 - Forward Power Loss Characteristics

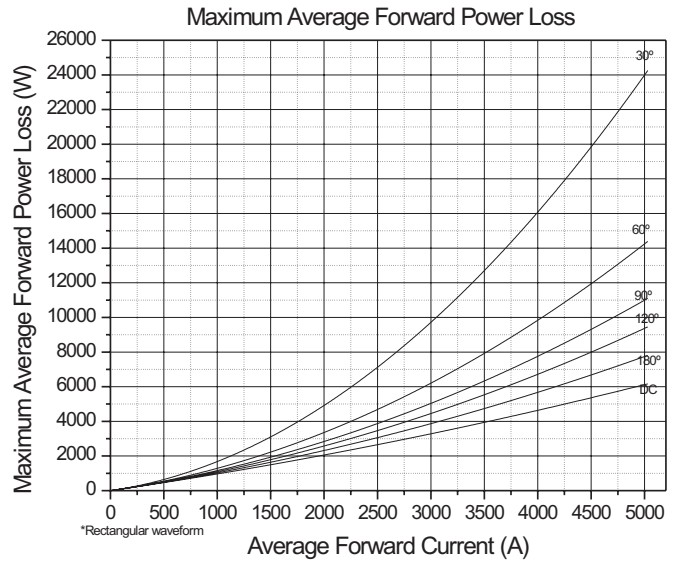


Fig. 4 - Forward Power Loss Characteristics

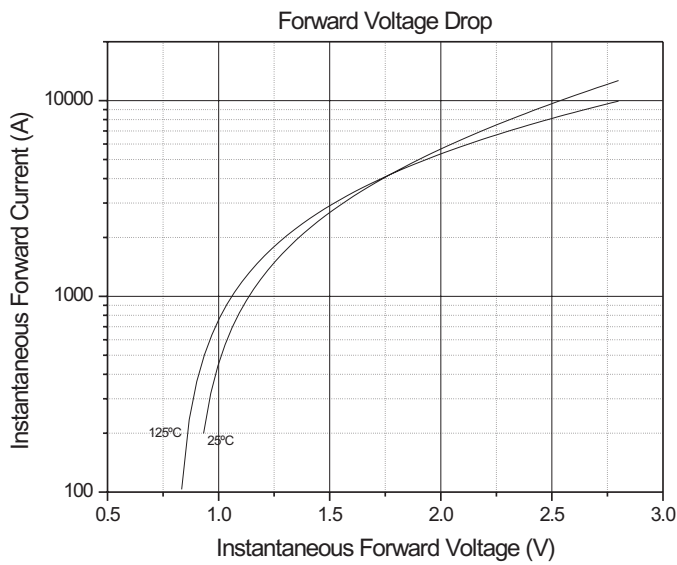


Fig. 5 - Forward Voltage Drop Characteristics

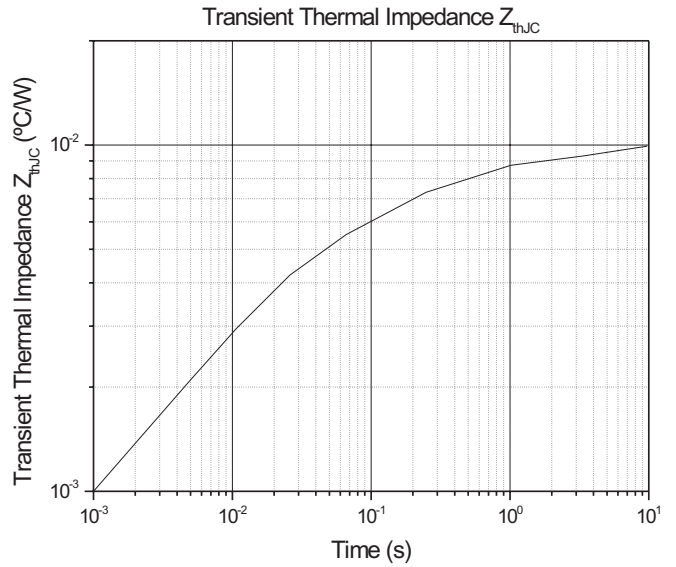
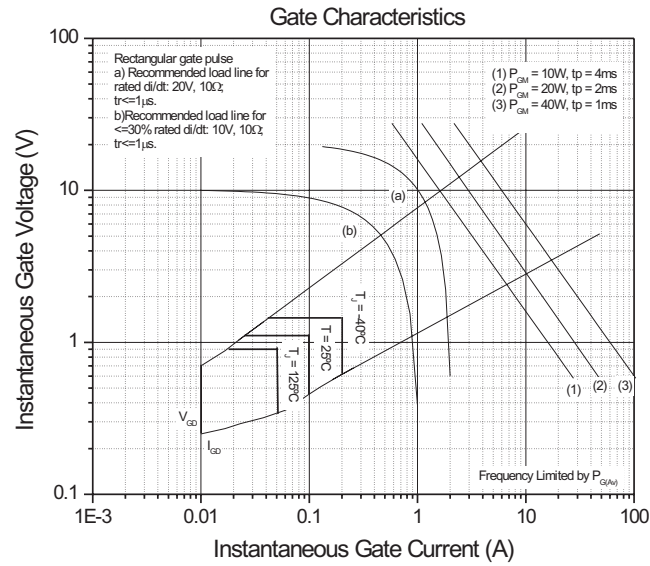


Fig. 6 - Transient Thermal Impedance Characteristics

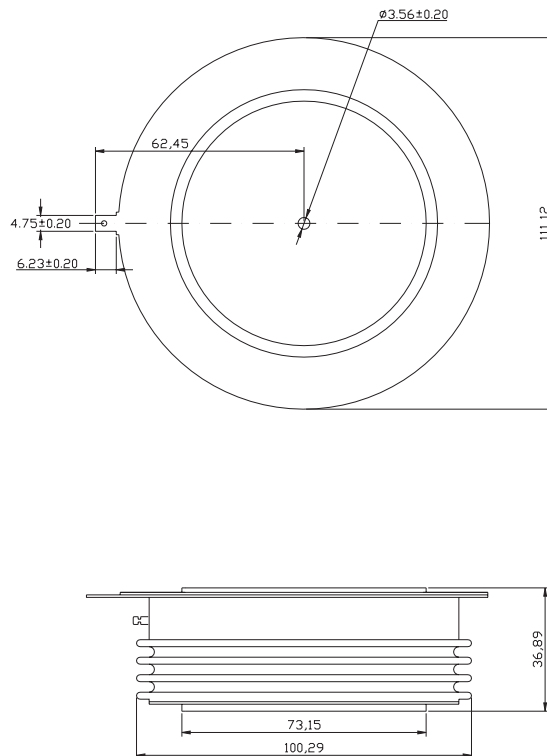


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**Fig. 7 - Gate Trigger Characteristics**

## TO-200AE



**Fig. 8 - Outline Characteristics**