



## A5N:1000.XXH

### VOLTAGE RATINGS

Part Number	V <sub>RRM</sub> , V <sub>R</sub> – (V) Max. rep. peak reverse voltage		V <sub>RSM</sub> , V <sub>R</sub> – (V) Max. non-rep. peak reverse voltage
	T <sub>J</sub> = 0 to 125°C	T <sub>J</sub> = -40 to 0°C	
	T <sub>J</sub> = 25 to 125°C		
A5N:1000.22H	2200	2200	2300
A5N:1000.24H	2400	2400	2500
A5N:1000.26H	2600	2600	2700
A5N:1000.28H	2800	2800	2900
A5N:1000.30H	3000	3000	3100
A5N:1000.32H	3200	3200	3300

### MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T <sub>J</sub> Junction Temperature	-40 to 125	°C	-
T <sub>stg</sub> Storage Temperature	-40 to 150	°C	-
I <sub>T(AV)</sub> Max. Av. current @ Max. T <sub>C</sub>	1000	A	180° half sine wave
	74	°C	
I <sub>T(RMS)</sub> Nom. RMS current	1600	A	-
I <sub>TSM</sub> Max. Peak non-rep. surge current	14000	A	50 Hz half cycle sine wave
	15000		60 Hz half cycle sine wave
I <sup>2</sup> t Max. I <sup>2</sup> t capability	937000	A <sup>2</sup> s	t = 10ms
	973000		t = 8.3 ms
I <sup>2</sup> t <sup>1/2</sup> Max. I <sup>2</sup> t <sup>1/2</sup> capability	46700	kA <sup>2</sup> s <sup>1/2</sup>	Initial T <sub>J</sub> = 125°C, no voltage applied after surge. I <sup>2</sup> t for time t <sub>x</sub> = I <sup>2</sup> t <sup>1/2</sup> * t <sub>x</sub> <sup>1/2</sup> . (0.1 < t <sub>x</sub> < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	300	A/μs	T <sub>J</sub> = 125°C, V <sub>D</sub> = V <sub>DRM</sub> , I <sub>TM</sub> = 3000A. Gate pulse: 20V, 20Ω, approximately 40% of non-repetitive value.
P <sub>GM</sub> Max. Peak gate power	200	W	t <sub>p</sub> = 40 μs
P <sub>G(AV)</sub> Max. Av. gate power	5	W	-
+I <sub>GM</sub> Max. Peak gate current	10	A	-
-V <sub>GM</sub> Max. Peak negative gate voltage	5	V	-
F Mounting Force	24500(5500) +- 10%	N(Lbf)	-



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### CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V <sub>TM</sub> peak on-state voltage	---	---	2.26	V	Initial T <sub>J</sub> = 25°C, 50-60Hz half sine, I <sub>beak</sub> = 3000A.
V <sub>F(TO)1</sub> Low-level threshold	---	---	1.31	V	T <sub>J</sub> = 125°C Av. power = V <sub>T(TO)</sub> * I <sub>T(AV)</sub> + r <sub>T</sub> * [I <sub>T(RMS)</sub> ] <sup>2</sup> , 180 Half Sine.
V <sub>F(TO)2</sub> High-level threshold	---	---	1.55		
r <sub>T1</sub> Low-level resistance	---	---	0.48	mΩ	Use low values for I <sub>TM</sub> < π rated I <sub>T(AV)</sub>
r <sub>T2</sub> High-level resistance	---	---	0.38		
I <sub>L</sub> Latching current	---	---	800	mA	T <sub>C</sub> = 125°C, 12V anode. Gate pulse: 10V, 20Ω, 100μs.
I <sub>H</sub> Holding current	---	---	400	mA	T <sub>C</sub> = 25°C, 12V anode. Initial IT = 15A.
t <sub>d</sub> Delay time	---	0.7	1.5	μs	T <sub>C</sub> = 25°C, V <sub>D</sub> = rated V <sub>DRM</sub> , 50A resistive load. Gate pulse: 10V, 20Ω, 20μs, 0.1μs rise time.
t <sub>q</sub> Turn-off time	---	125	250	μs	T <sub>J</sub> = 125°C, I <sub>TM</sub> = 1000A, di/dt = 25A/μs, V <sub>R</sub> = -50V. dv/dt = 20 V/μs lin. To 80% rated V <sub>DRM</sub> . Gate: 0V, 100Ω.
t <sub>q(diode)</sub> Turn-off time with feedback diode	---	---	50	μs	T <sub>J</sub> = 125°C, I <sub>TM</sub> = 1000A, di/dt = 25A/μs, V <sub>R</sub> = 1V. dv/dt = 600 V/μs lin. To 40% rated V <sub>DRM</sub> . Gate: 0V, 100Ω.
I <sub>RM(REC)</sub> Recovery current	---	93	---	A	T <sub>J</sub> = 125°C, I <sub>TM</sub> = 1000A, diR/dt = 25A/μs.
Q <sub>RR</sub> Recovered charge	---	166	---	μC	
dv/dt Critical rate-of-rise of off-state voltage	300	---	1000	V/μs	T <sub>J</sub> = 125°C. Exp. to 100% or lin. Higher dv/dt values available.
	---	---	300		T <sub>J</sub> = 125°C, Exp. To 67% V <sub>DRM</sub> , gate open.
I <sub>RM</sub> , I <sub>DM</sub> Peak reverse and off-state current	---	15	75	mA	T <sub>J</sub> = 125°C, Rated V <sub>RRM</sub> and V <sub>DRM</sub> , gate open.
I <sub>GT</sub> DC gate current to trigger	---	40	300	mA	T <sub>C</sub> = -40°C T <sub>C</sub> = 25°C +6V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
	---	20	150		
V <sub>GT</sub> DC gate voltage to trigger	0.3	---	5	V	T <sub>C</sub> = -40°C T <sub>C</sub> = 25°C
	0.3	---	3		
V <sub>GD</sub> DC gate voltage not to trigger	---	---	0.200	V	T <sub>C</sub> = 25°C, Max. Value which will not trigger with rated V <sub>DRM</sub> anode-to-cathode.
R <sub>thJC</sub> Thermal resistance, junction-to-case	---	---	0.025	°C/W	DC operation, double side cooled.
	---	---	0.025	°C/W	180° sine wave, double side cooled.
	---	---	0.027	°C/W	120° rectangular wave, double side cooled.
R <sub>thCS</sub> Thermal resistance, case-to-sink	---	---	0.010	°C/W	Mtg. Surface smooth, flat and greased. Single side cooled. For double side, divide by 2.
wt Weight	---	460(16.0)	---	g(oz.)	---
Case Style	---	TO-200AD	---	JEDEC	---



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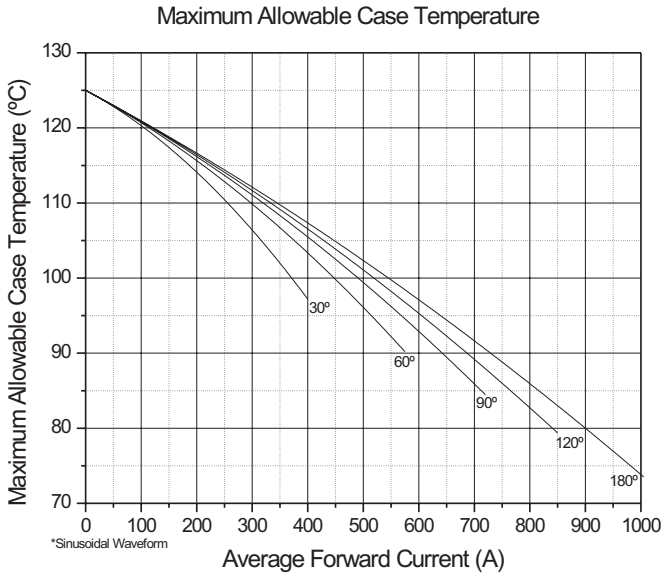


Fig. 1 - Current Ratings Characteristics

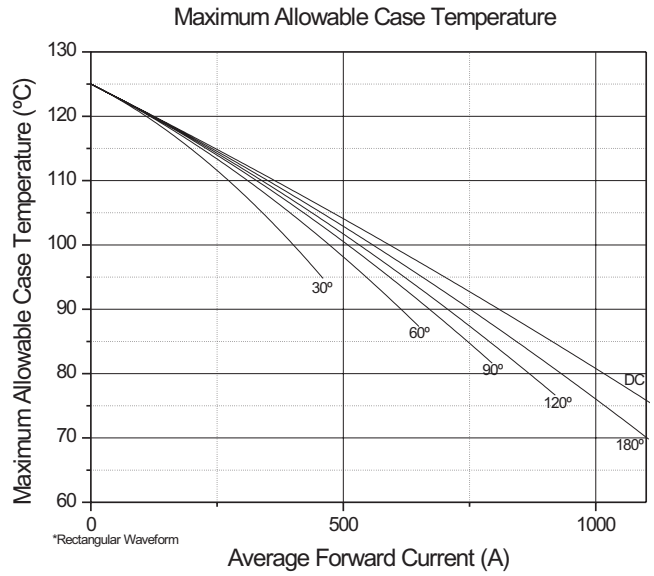


Fig. 2 - Current Ratings Characteristics

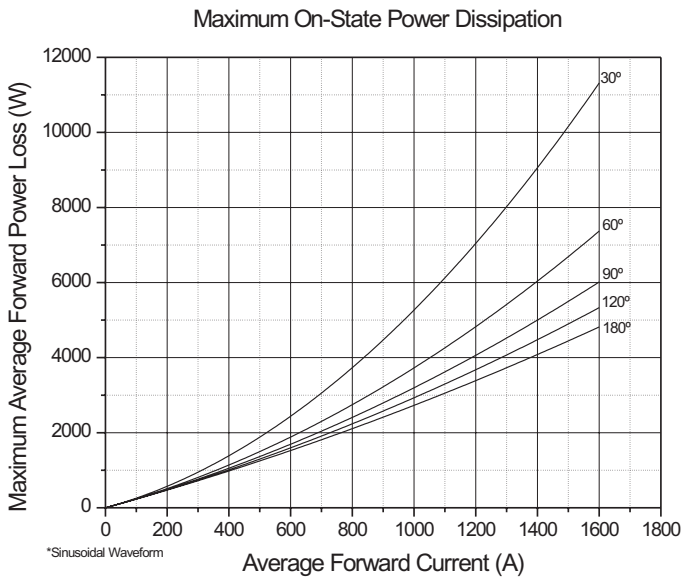


Fig. 3 - On-state Power Loss Characteristics

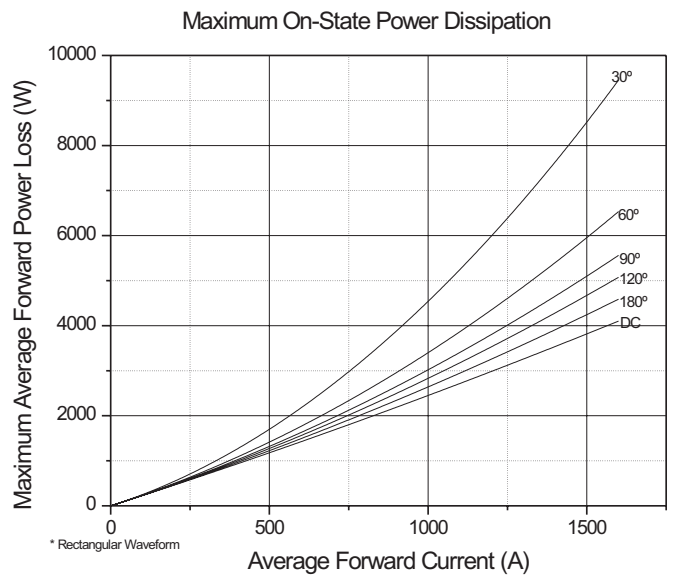


Fig. 4 - On-state Power Loss Characteristics



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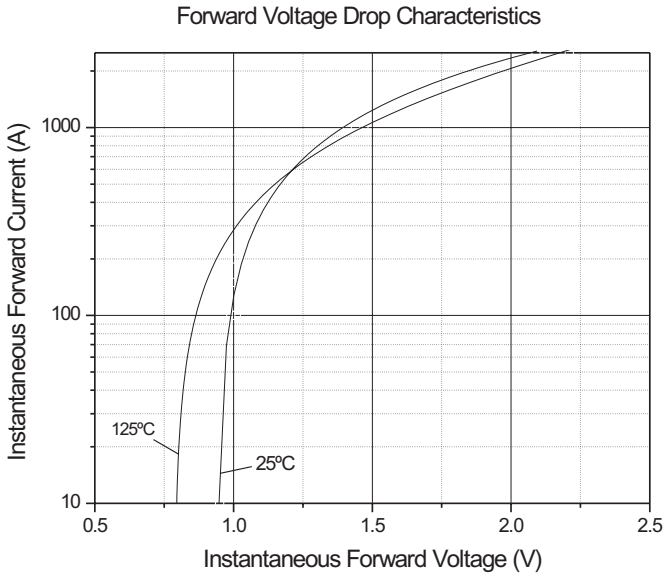


Fig. 5 - Forward Voltage Drop Characteristics

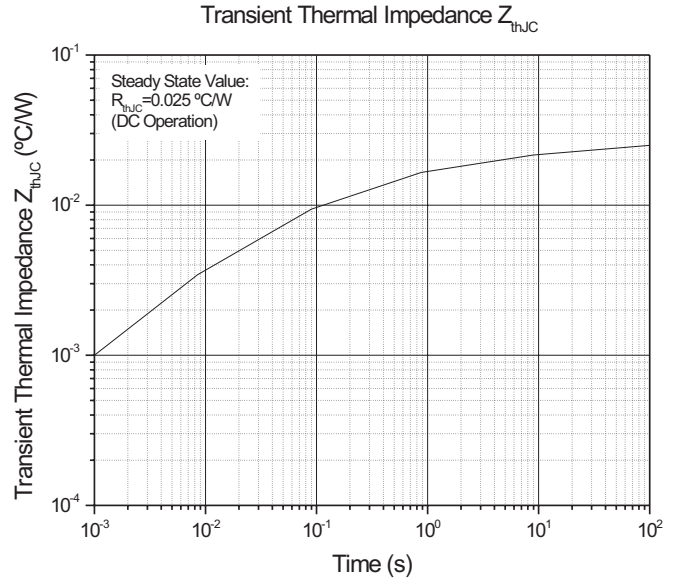


Fig. 6 - Transient Thermal Impedance  $Z_{thJC}$  Characteristics

## TO-200AD

