



## A3L:55TT.XXI

### VOLTAGE RATINGS

Part Number	V <sub>RRM</sub> , V <sub>R</sub> (V) Max. rep. peak reverse voltage		V <sub>RSM</sub> , V <sub>R</sub> (V) Max. non- rep. peak reverse voltage
	T <sub>J</sub> = 0 to 125°C	T <sub>J</sub> = -40 to 0°C	T <sub>J</sub> = 25 to 125°C
	A3L:55TT.02I	200	200
A3L:55TT.04I	400	400	500
A3L:55TT.06I	600	600	700
A3L:55TT.08I	800	800	900
A3L:55TT.10I	1000	1000	1100
A3L:55TT.12I	1200	1200	1300
A3L:55TT.14I	1400	1330	1500
A3L:55TT.16I	1600	1520	1700

### MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T <sub>J</sub> Junction Temperature	-40 to 125	°C	-
T <sub>stg</sub> Storage Temperature	-40 to 150	°C	-
I <sub>F(AV)</sub> Max. Av. current @ Max. T <sub>C</sub>	55	A	180° half sine wave
	85	°C	
I <sub>F(RMS)</sub> Nom. RMS current	122	A	-
I <sub>FSM</sub> Max. Peak non-rep. surge current	1.1	kA	50 Hz half cycle sine wave Initial T <sub>J</sub> = 125°C, rated V <sub>RRM</sub> applied after surge.
	1.2		60 Hz half cycle sine wave
	1.26		50 Hz half cycle sine wave Initial T <sub>J</sub> = 125°C, no voltage applied after surge.
	1.37		60 Hz half cycle sine wave
I <sup>2</sup> t Max. I <sup>2</sup> t capability	6.29	kA <sup>2</sup> s	t = 10ms Initial T <sub>J</sub> = 125°C, rated V <sub>RRM</sub> applied after surge.
	6.85		t = 8.3 ms
	7.17		t = 10ms Initial T <sub>J</sub> = 125°C, no voltage applied after surge.
	7.81		t = 8.3 ms
I <sup>2</sup> t <sup>1/2</sup> Max. I <sup>2</sup> t <sup>1/2</sup> capability	85.6	kA <sup>2</sup> s <sup>1/2</sup>	Initial T <sub>J</sub> = 125°C, no voltage applied after surge. I <sup>2</sup> t for time t <sub>x</sub> = I <sup>2</sup> t <sup>1/2</sup> * t <sub>x</sub> <sup>1/2</sup> . (0.1 < t <sub>x</sub> < 10ms).
di/dt Max. Non-repetitive rate-of- rise current	150	A/μs	T <sub>J</sub> = 125°C, V <sub>D</sub> = V <sub>DRM</sub> , I <sub>TM</sub> = 1600A. Gate pulse: 20V, 20Ω, 10μs, 0.5μs rise time, Max. repetitive di/dt is approximately 40% of non-repetitive value.
P <sub>GM</sub> Max. Peak gate power	10	W	tp < 5 ms
P <sub>G(AV)</sub> Max. Av. gate power	2.5	W	-
+I <sub>GM</sub> Max. Peak gate current	150	mA	tp < 5 ms
-V <sub>GM</sub> Max. Peak negative gate voltage	2	V	-
F Mounting Force	3(5)	N.m	Upper connectors(Heatsink)



## A3L:55TT.XXI

### CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$V_{TM}$ peak on-state voltage	---	---	1.47	V	Initial $T_J = 25^\circ\text{C}$ , 50-60Hz half sine, $I_{peak} = 173\text{A}$ .
$V_{T(TO)}$ Threshold voltage	---	---	0.89	V	$T_J = 125^\circ\text{C}$ Av. power = $V_{T(TO)} * I_{T(AV)} + r_T * [I_{T(RMS)}]^2$ , 180 Half Sine.
$r_T$ Slope resistance	---	---	3.68	m $\Omega$	Use low values for $I_{TM} < \pi$ rated $I_{T(AV)}$
$I_L$ Latching current	---	---	400	mA	$T_C = 125^\circ\text{C}$ , 12V anode. Gate pulse: 10V, 20 $\Omega$ , 100 $\mu\text{s}$ .
$I_H$ Holding current	---	---	200	mA	$T_C = 25^\circ\text{C}$ , 12V anode. Initial $I_T = 15\text{A}$ .
$t_d$ Delay time	---	0.7	1.5	$\mu\text{s}$	$T_C = 25^\circ\text{C}$ , $V_D = V_{DRM}$ , 50A resistive load. Gate pulse: 10V, 20 $\Omega$ , 10 $\mu\text{s}$ , 1 $\mu\text{s}$ rise time.
$t_q$ Turn-off time	---	125	200	$\mu\text{s}$	$T_J = 125^\circ\text{C}$ , $I_{TM} = 500\text{A}$ , $di/dt = 25\text{A}/\mu\text{s}$ , $V_R = 50\text{V}$ . $dv/dt = 20\text{V}/\mu\text{s}$ lin. to rated $V_{DRM}$ . Gate: 0V, 100 $\Omega$ .
$dv/dt$ Critical rate-of-rise of off-state voltage	80	140	---	V/ $\mu\text{s}$	$T_J = 125^\circ\text{C}$ . Exp. to 100% or lin. Higher $dv/dt$ values To 80% $V_{DRM}$ , gate open. available.
	---	---	500		$T_J = 125^\circ\text{C}$ , Exp. To 67% $V_{DRM}$ , gate open.
$I_{RM}$ , $I_{DM}$ Peak reverse and off-state current	---	10	15	mA	$T_J = 125^\circ\text{C}$ , Rated $V_{RRM}$ and $V_{DRM}$ , gate open.
$I_{GT}$ DC gate current to trigger	---	---	300	mA	$T_C = -40^\circ\text{C}$
	50	80	150		$T_C = 25^\circ\text{C}$ +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
$V_{GT}$ DC gate voltage to trigger	4	---	---	V	$T_C = -40^\circ\text{C}$
	2	---	2.5		$T_C = 25^\circ\text{C}$
$V_{GD}$ DC gate voltage not to trigger	---	---	0.2	V	$T_C = 25^\circ\text{C}$ , Max. Value which will not trigger with rated $V_{DRM}$ anode.
$R_{thJC}$ Thermal resistance, junction-to-case	---	---	0.25	$^\circ\text{C}/\text{W}$	DC operation, single side cooled.
	---	---	0.261	$^\circ\text{C}/\text{W}$	180 sine wave, single side cooled.
	---	---	0.273	$^\circ\text{C}/\text{W}$	120 rectangular wave, single side cooled.
$R_{thCS}$ Thermal resistance, case-to-sink	---	---	0.1	$^\circ\text{C}/\text{W}$	Mtg. Surface smooth, flat and greased. Single side cooled.
wt Weight	---	110(4)	---	g(oz.)	---
Case Style	TO-240AA			JEDEC	---

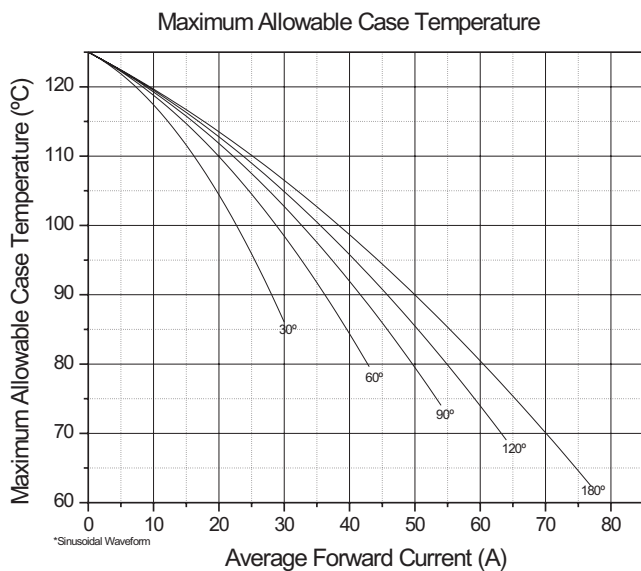


Fig. 1 - Current Ratings Characteristics

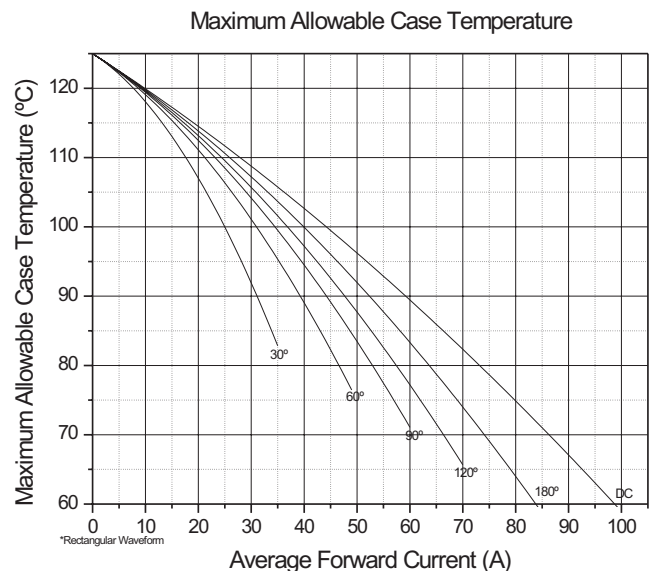
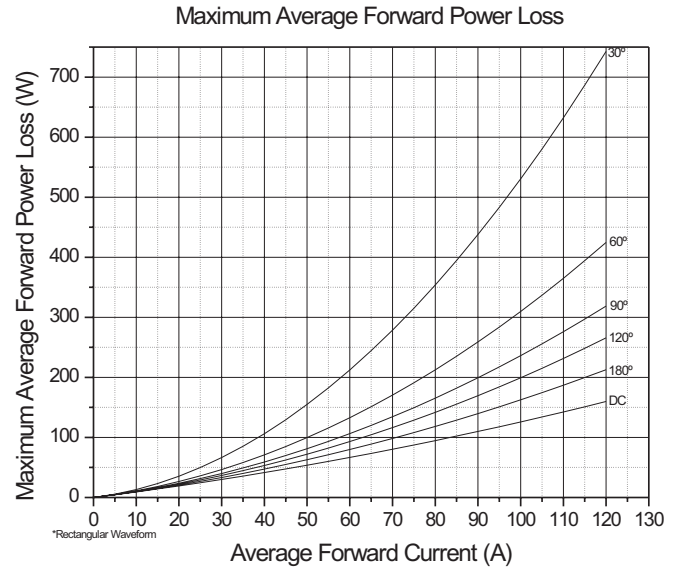
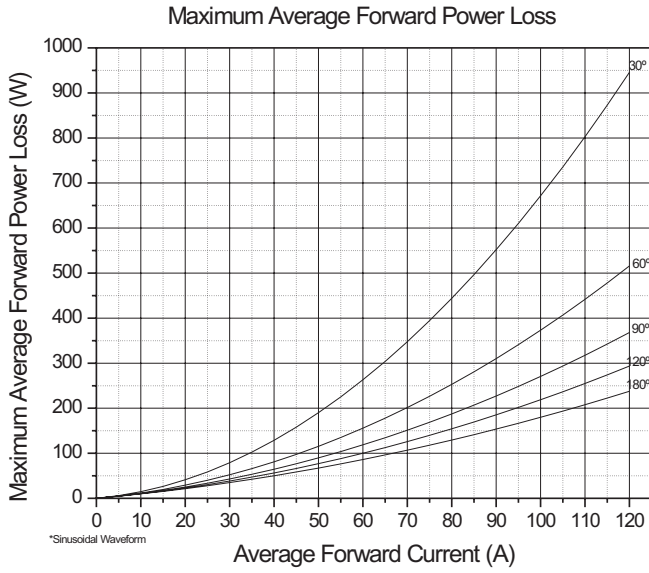


Fig. 2 - Current Ratings Characteristics

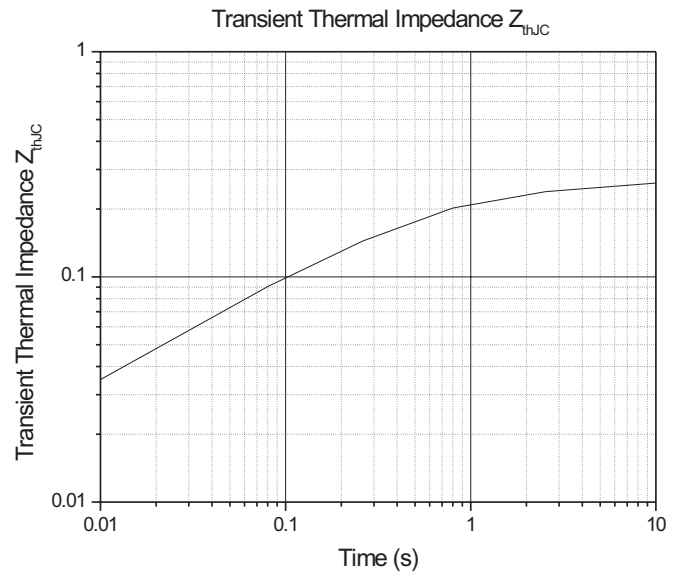
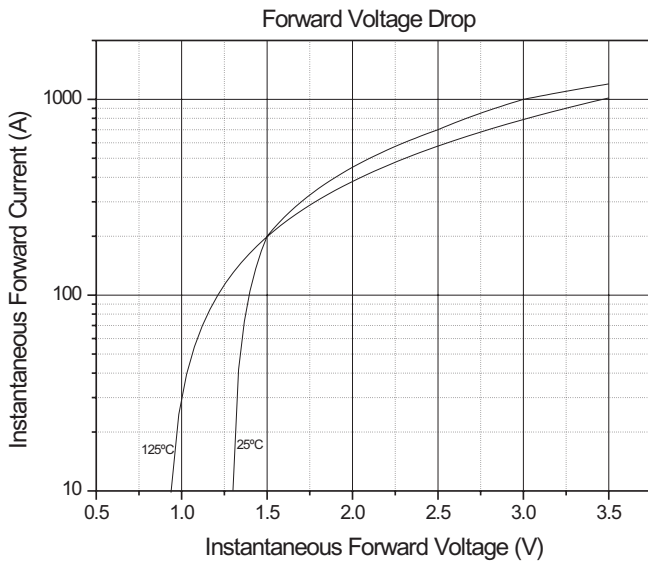


# A3L:55TT.XXI



**Fig.3 -Forward Power Loss Characteristics**

**Fig. 4 - Forward Power Loss Characteristics**

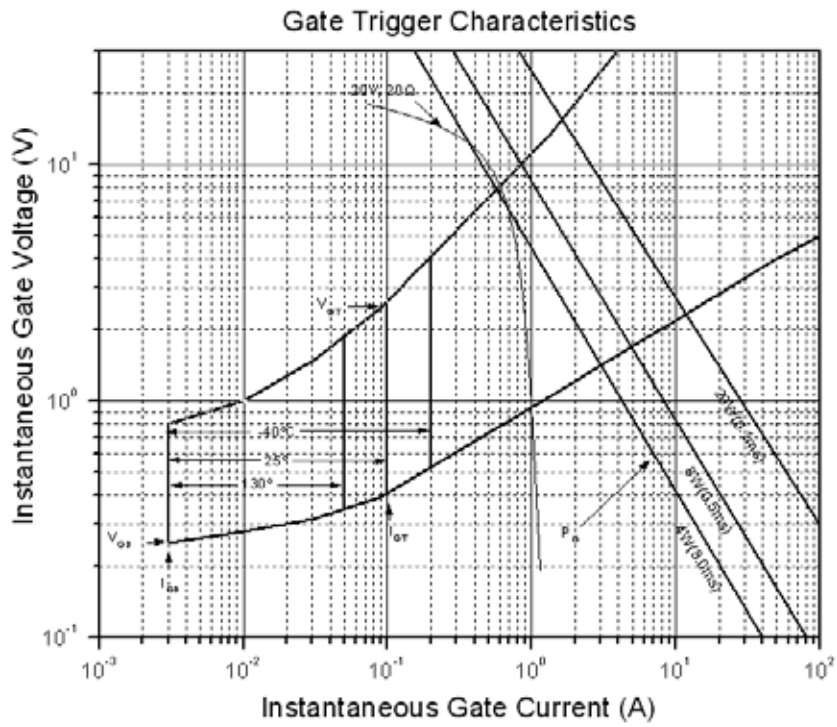


**Fig. 5 - Forward Voltage Drop Characteristics**

**Fig. 6 - Transient Thermal Impedance**

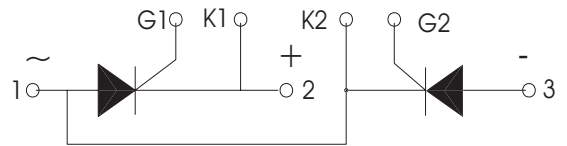
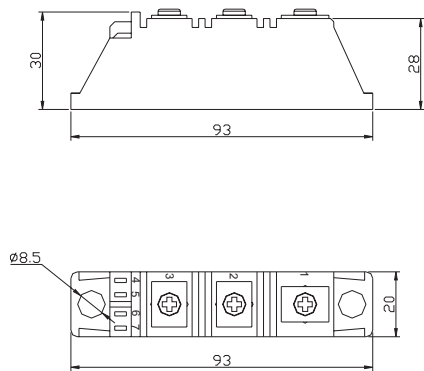


# A3L:55TT.XXI



**Fig. 7 - Gate Trigger Characteristics**

## TO-240AA



**Fig. 8 - Outline Characteristics**

**Fig. 9 - Circuit Layout**