



A3L:250TT.XXH

VOLTAGE RATINGS

Part Number	V _{RRM} , V _R (V) Max. rep. peak reverse voltage		V _{RSM} , V _R (V) Max. non- rep. peak reverse voltage
	T _J = 0 to 125 °C	T _J = -40 to 0 °C	T _J = 25 to 125 °C
	A3L:250TT.02H	200	200
A3L:250TT.04H	400	400	500
A3L:250TT.06H	600	600	700
A3L:250TT.08H	800	800	900
A3L:250TT.10H	1000	1000	1100
A3L:250TT.12H	1200	1200	1300
A3L:250TT.14H	1400	1330	1500
A3L:250TT.16H	1600	1520	1700

MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T _J Junction Temperature	-40 to 125	°C	-
T _{stg} Storage Temperature	-40 to 150	°C	-
I _{F(AV)} Max. Av. current @ Max. T _C	250	A	180° half sine wave
	85	°C	
I _{F(RMS)} Nom. RMS current	555	A	-
I _{FSM} Max. Peak non-rep. surge current	7.16	kA	50 Hz half cycle sine wave Initial T _J = 125°C, rated V _{RRM} applied after surge.
	7.81		60 Hz half cycle sine wave
	8.17		50 Hz half cycle sine wave Initial T _J = 125°C, no voltage applied after surge.
	8.9		60 Hz half cycle sine wave
I ² t Max. I ² t capability	265	kA ² s	t = 10ms Initial T _J = 125°C, rated V _{RRM} applied after surge.
	289		t = 8.3 ms
	302		t = 10ms Initial T _J = 125°C, no voltage applied after surge.
	329		t = 8.3 ms
I ² t ^{1/2} Max. I ² t ^{1/2} capability	3610	kA ² s ^{1/2}	Initial T _J = 125°C, no voltage applied after surge. I ² t for time t _x = I ² t ^{1/2} * t _x ^{1/2} . (0.1 < t _x < 10ms).
di/dt Max. Non-repetitive rate-of-rise current	500	A/μs	T _J = 125°C, V _D = V _{DRM} , I _{TM} = 1600A. Gate pulse: 20V, 20Ω, 10μs, 0.5μs rise time, Max. repetitive di/dt is approximately 40% of non-repetitive value.
P _{GM} Max. Peak gate power	10	W	tp < 5 ms
P _{G(AV)} Max. Av. gate power	3	W	-
+I _{GM} Max. Peak gate current	150	mA	tp < 5 ms
-V _{GM} Max. Peak negative gate voltage	2	V	-
F Mounting Force	3(5)	N.m	Upper connectors(Heatsink)



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CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM} peak on-state voltage	---	---	1.37	V	Initial $T_J = 25^\circ\text{C}$, 50-60Hz half sine, $I_{peak} = 785\text{A}$.
$V_{T(To)}$ Threshold voltage	---	---	0.89	V	$T_J = 125^\circ\text{C}$ Av. power = $V_{T(To)} * I_{T(AV)} + r_T * [I_{T(RMS)}]^2$, 180 Half Sine.
r_T Slope resistance	---	---	0.61	m Ω	Use low values for $I_{TM} < \pi$ rated $I_{T(AV)}$
I_L Latching current	---	---	200	mA	$T_C = 125^\circ\text{C}$, 12V anode. Gate pulse: 10V, 20 Ω , 100 μs .
I_H Holding current	---	---	500	mA	$T_C = 25^\circ\text{C}$, 12V anode. Initial $I_T = 15\text{A}$.
t_d Delay time	---	0.7	1.5	μs	$T_C = 25^\circ\text{C}$, $V_D = V_{DRM}$, 50A resistive load. Gate pulse: 10V, 20 Ω , 10 μs , 1 μs rise time.
t_q Turn-off time	---	125	200	μs	$T_J = 125^\circ\text{C}$, $I_{TM} = 500\text{A}$, $di/dt = 25\text{A}/\mu\text{s}$, $V_R = 50\text{V}$. $dv/dt = 20\text{V}/\mu\text{s}$ lin. to rated V_{DRM} . Gate: 0V, 100 Ω .
dv/dt Critical rate-of-rise of off-state voltage	80	140	---	V/ μs	$T_J = 125^\circ\text{C}$. Exp. to 100% or lin. Higher dv/dt values To 80% V_{DRM} , gate open. available. $T_J = 125^\circ\text{C}$, Exp. To 67% V_{DRM} , gate open.
I_{RM} , I_{DM} Peak reverse and off-state current	---	10	50	mA	$T_J = 125^\circ\text{C}$, Rated V_{RRM} and V_{DRM} , gate open.
I_{GT} DC gate current to trigger	---	---	300	mA	$T_C = -40^\circ\text{C}$ $T_C = 25^\circ\text{C}$ +12V anode-to-cathode. For recommended gate drive see "Gate Characteristics" figure.
V_{GT} DC gate voltage to trigger	4	---	---	V	$T_C = -40^\circ\text{C}$ $T_C = 25^\circ\text{C}$
V_{GD} DC gate voltage not to trigger	---	---	0.3	V	$T_C = 25^\circ\text{C}$, Max. Value which will not trigger with rated V_{DRM} anode.
R_{thJC} Thermal resistance, junction-to-case	---	---	0.07	$^\circ\text{C}/\text{W}$	DC operation, single side cooled.
	---	---	0.071	$^\circ\text{C}/\text{W}$	180 sine wave, single side cooled.
	---	---	0.075	$^\circ\text{C}/\text{W}$	120 rectangular wave, single side cooled.
R_{thCS} Thermal resistance, case-to-sink	---	---	0.02	$^\circ\text{C}/\text{W}$	Mtg. Surface smooth, flat and greased. Single side cooled.
wt Weight	---	500(18)	---	g(oz.)	---

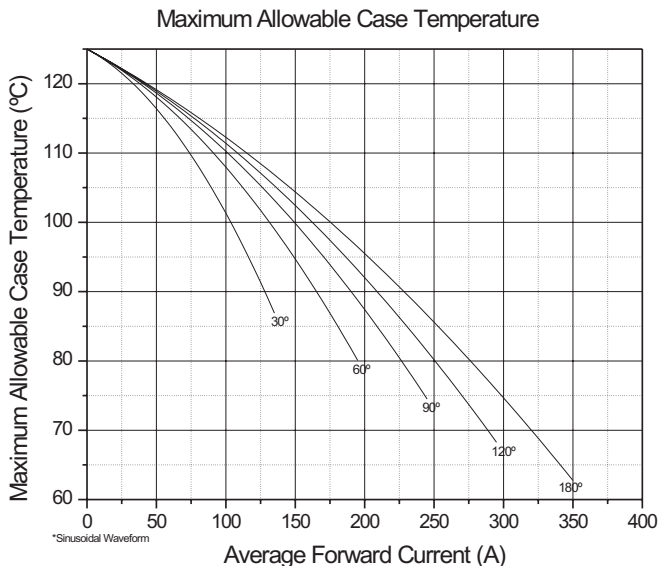


Fig. 1 - Current Ratings Characteristics

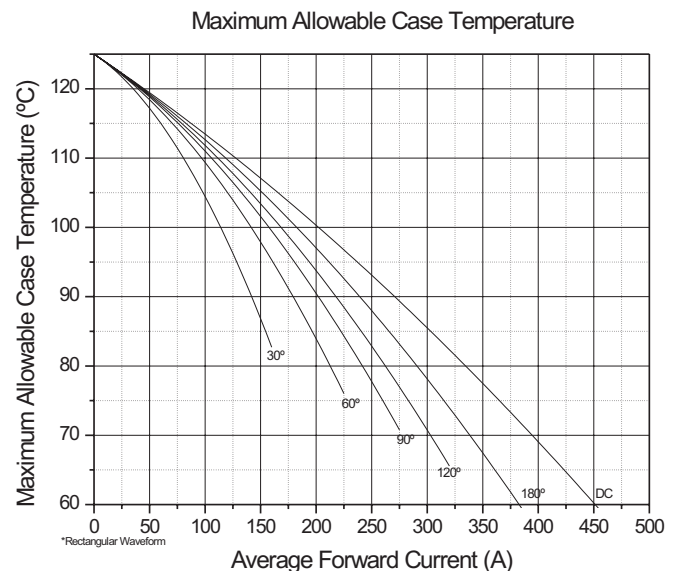


Fig. 2 - Current Ratings Characteristics



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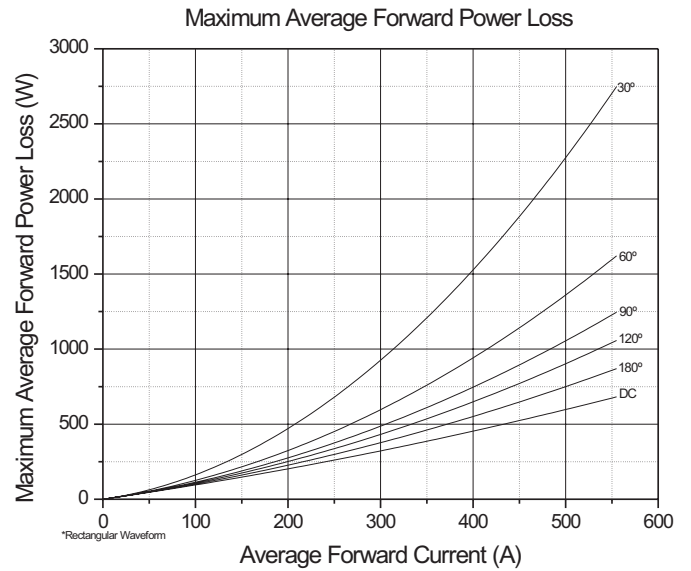
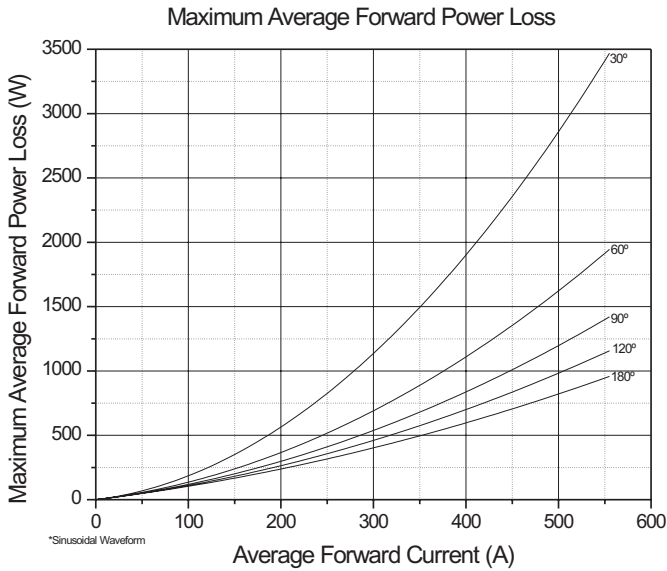


Fig.3 -Forward Power Loss Characteristics

Fig. 4 - Forward Power Loss Characteristics

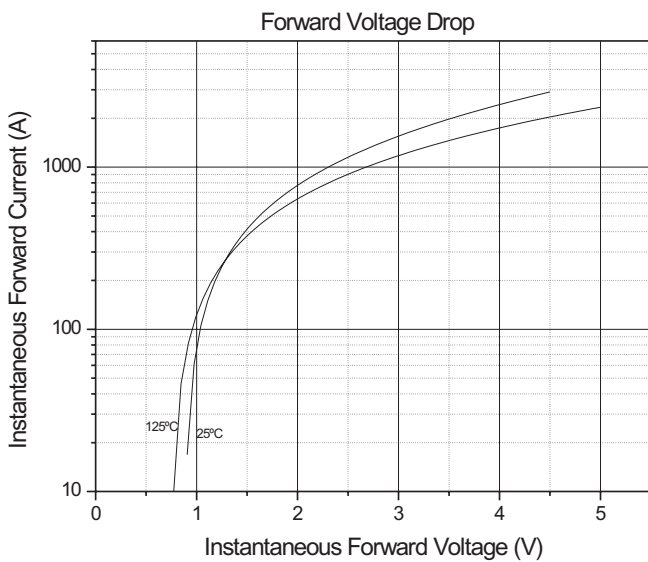


Fig. 5 - Forward Voltage Drop Characteristics

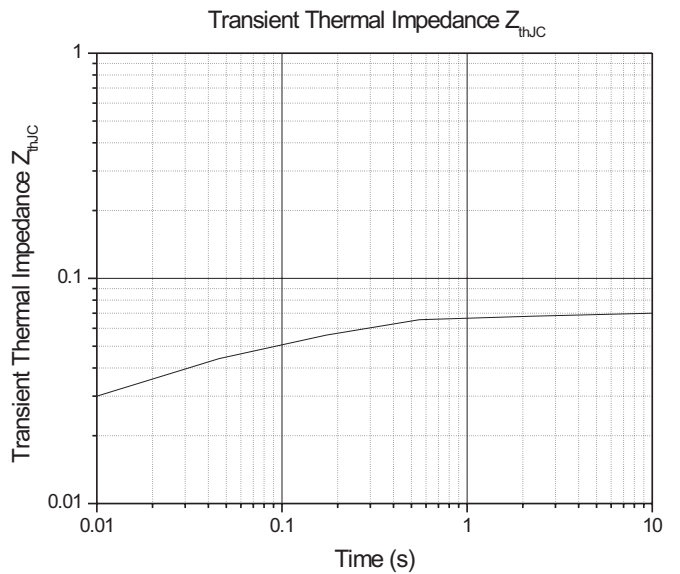


Fig. 6 - Transient Thermal Impedance



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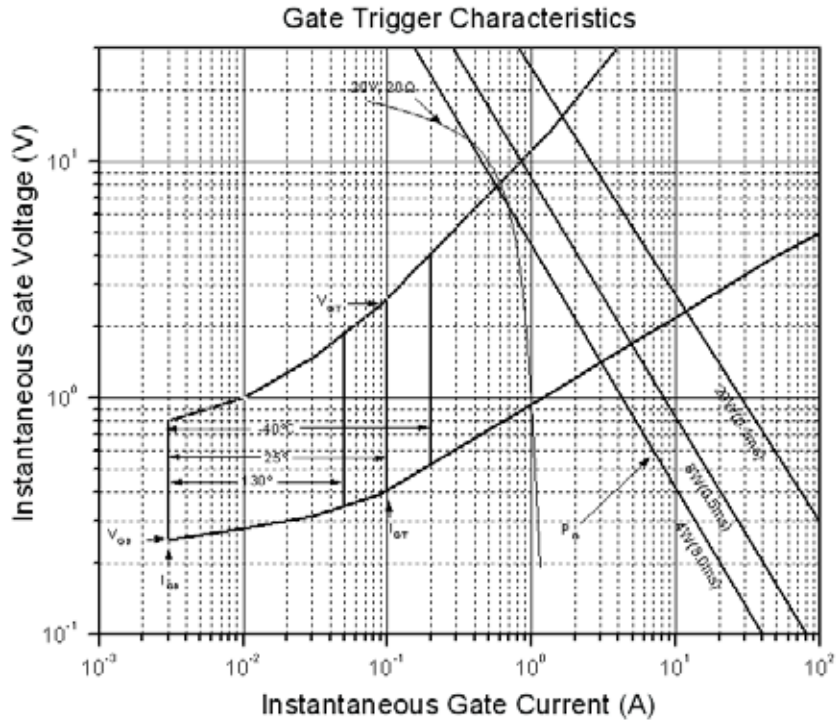


Fig. 7 - Gate Trigger Characteristics

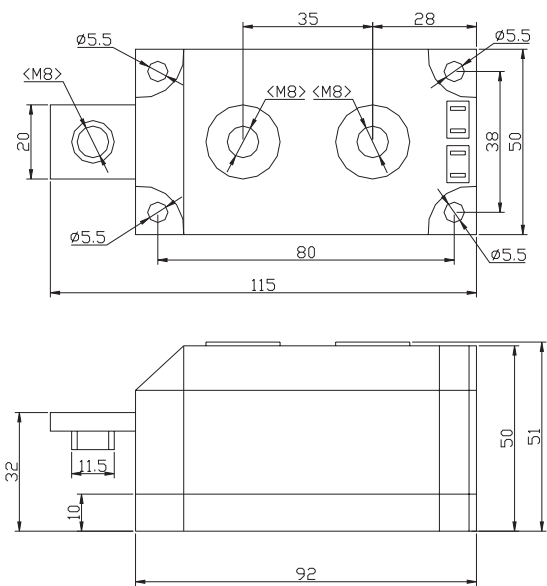


Fig. 8 - Outline Characteristics

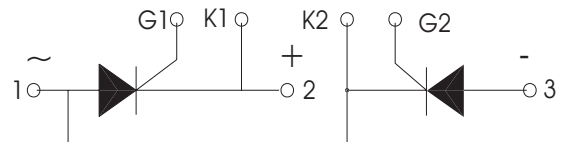


Fig. 9 - Circuit Layout